REMARKS

Claims 15-29 are pending in this application. Claims 1-14 were previously withdrawn. Claim 30 has been canceled in the present amendment. In view of the remarks contained herein, Applicants respectfully request reconsideration of the claims.

I. REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 24-30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,705,298 to Knoedl, Jr (hereinafter "*Knoedl*").

A. Improper Rejections

The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity. MPEP § 706. In the pending Office Action, the Examiner failed to address or apply the teachings of the cited references to each individual claim. Instead, the Examiner merely provides a narrative describing teachings similar to those of the cited references and stating that those teachings anticipate the claims under examination. Moreover, the Examiner completely failed to provide specific cites to the cited references to support his contentions. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. 37 C.F.R. § 1.104(c)(2). This type of examination fails to provide the Applicant an opportunity to reply completely at the earliest opportunity. Applicant, therefore, respectfully requests the Examiner to properly examine the present application and provide Applicant a fair opportunity to respond.

B. Failure to Teach All Elements

To anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim. *See* M.P.E.P. § 2131. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Moreover,

"[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989).

Claim 25 requires, "depositing a material layer over the photoresist layer ...." The Examiner asserts that *Knoedl* completely anticipates claim 25, yet fails to provide either any specific citation from *Knoedl* that describes depositing a material layer over the photoresist layer, or any statement that *Knoedl* even teaches this limitation. In fact, *Knoedl* does not teach such limitation. *Knoedl* teaches that holographic transform information is written or recorded onto a planar side of a three-dimensional conformal photo mask to form a holograph and then photoresist is coated on the three-dimensional side of the mask. Col. 4, lns 59-64. Coherent light is then irradiated through the holograph and a mask to form a hologram that defines the features to be imaged onto the photoresist. Col 4. lns 65-67. The material under the exposed photoresist is then removed to form the three-dimensional impressions. Col. 5, lns 1-8. There are no further teachings of depositing a material layer over the photoresist. Thus, *Knoedl* does not teach each and every limitation of claim 25.

Claims 26–29 depend directly from independent claim 25 and therefore inherit all the elements of claim 25. Accordingly, claims 26–29 are allowable for at least the reasons discussed above. Applicant, therefore, respectfully requests that the rejection of claims 25–29 likewise be withdrawn.

C. Product-By-Process Claims

Claim 24 is written as product-by-process claims. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698 (Fed. Cir. 1985). The Examiner should consider the structure implied by the process steps when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive

structural characteristics to the final product. *See. e.g., In re Garnero*, 412 F.2d 276, 279 (CCPA 1979). In the present examination, the Examiner has not properly compared the structures defined both in the cited reference and in the claimed invention.

Claim 24 claims "[a] semiconductor device patterned according to the method of Claim 23. Claim 23 defines the method of claim 15 in which "the target comprises a semiconductor wafer." Thus, in order to properly examine claim 24, the Examiner must use the product created by the method of claim 15 in which the target is a semiconductor wafer.

Claim 15 provides, "[a] method for patterning a target ...", in which the target for this analysis is a semiconductor wafer, as per claim 23. Thus, the product of claim 24 is a semiconductor wafer having a pattern. Claim 15 further requires:

> the target having a top surface, the target top surface having a material layer disposed thereon, a first photoresist layer disposed over the material layer, a transparent spacer material disposed over the first photoresist layer, and a second photoresist layer disposed over the spacer material ...."

Thus, the semiconductor device of claim 24 requires a semiconductor wafer which has a material layer, a first photoresist layer on top of that, a transparent spacer material on top of the first photoresist layer, and a second photoresist layer on to of the transparent spacer.

Finally, claim 15 requires, "patterning the second photoresist layer of the target with a holographic fringe representation of an image." Thus, the semiconductor device of claim 24 has the layered structure as described above, with a pattern having been etched in the second photoresist layer.

As noted above, *Knoedl* describes a single photoresist layer in which a pattern is etched into using a hologram. It does not teach a material layer, followed by a first photoresist layer, followed by a transparent spacer layer, followed by a second photoresist layer with the pattern etched into it from the holographic fringe representation of an image, as required by claim 15. Therefore, *Knoedl* does not teach each and every limitation of the invention claimed in claim 24. Applicant, therefore, respectfully requests that the rejection of claim 24 be withdrawn.

II. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 15-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2003/0124437 to Taniguchi (hereinafter "*Taniguchi*") and U.S. Patent No. 5,504,596 to Goto, *et al.* (hereinafter "*Goto*").

To establish a prima facie case for obviousness under 35 U.S.C. § 103(a), three basic criteria must be satisfied. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the applied art must teach or suggest all the claim elements. M.P.E.P. § 2143. Without conceding any other criteria, Applicant respectfully asserts that the applied references do not teach or suggest all elements of the claims.

A. Improper Rejections

As noted above, the Examiner has improperly provided his rejections to Applicant. The Examiner has summarized some of Applicant's claims and then provided narrative summaries of the cited references (without specific citation) in comparison. Applicant is entitled to a fair opportunity to respond to the Examiner's rejections, and, thus, respectfully request the Examiner to provide a proper examination.

B. Claims 15-23

Claim 15 requires:

> the target having a top surface, the target top surface having a material layer disposed thereon, a first photoresist layer disposed over the material layer, a transparent spacer material disposed over the first photoresist layer, and a second photoresist layer disposed over the spacer material ...."

The Examiner admits that *Taniguchi* does not teach the multiple layers required by claim 15, but offers *Goto* to cure this deficiency. In supporting the combination, the Examiner states that:

> It would have been obvious to one having ordinary skill in the art to take the teaching of Taniguchi and combine them with the teachings of Goto et al. in order to make the claimed invention because it is well known in the art to use multiple layers when using holographic exposure due to the need for combining images on a substrate. Office Action, p. 6.

Without commenting on the propriety of the proposed combination, Applicant reminds the Examiner that claim 15 does ***not*** recite "multiple layers." Claim 15 requires a target having a material layer on its top surface, a first photoresist layer on top of the material layer, a transparent spacer material on top of the first photoresist layer, and a second photoresist layer on to of the transparent spacer. While the specific layers required by claim 15 amount to "multiple layers," it is not sufficient to render claim 15 unpatentable under 35 U.S.C. 103(a) by merely finding a reference that recites "multiple layers," without those multiple layers corresponding exactly to the specific layers recited in claim 15. *Goto* does not teach or even suggest a target having a material layer on its top surface, a first photoresist layer on top of the material layer, a transparent spacer material on top of the first photoresist layer, and a second photoresist layer on to of the transparent spacer.

In fact, Applicant has not been able to find any statements in *Goto* that teach or suggest multiple layers (other than the resist applied to the surface of the wafer 5 – Col. 37). The Examiner generally and vaguely directs Applicant to the claims in support of his rejection. However, none of the three claims teaches multiple layers, let alone the specific multiple layers arranged in the manner required by claim 15. Thus, the combined teaching of *Taniguchi* and *Goto* fail to teach or suggest each and every limitation of the claimed invention.

Claims 16–23 depend directly from independent claim 15 and therefore inherit all the elements of claim 15. Accordingly, claims 16–23 are allowable for at least the reasons discussed above. Applicant, therefore, respectfully requests that the rejection of claims 15–23 likewise be withdrawn.

C. Claim 24

As noted above, claim 24 is written as product-by-process claims. Applicant contends that the Examiner has not properly compared the structures defined both in the cited reference and in the claimed invention.

Claim 24 claims "[a] semiconductor device patterned according to the method of Claim 23. Claim 23 defines the method of claim 15 in which "the target comprises a semiconductor wafer." Thus, in order to properly examine claim 24, the Examiner must use the product created by the method of claim 15 in which the target is a semiconductor wafer.

As noted above, the combined teachings of *Taniguchi* and *Goto* fail to teach each and every limitation of claim 15. Because claim 24 provides for a semiconductor device (claim 23) patterned according to the method of claim 15, the semiconductor device product resulting from the method of claim 15 also is patentable over the combined teachings. Neither *Taniguchi* nor *Goto*, either alone or in combination teach a material layer, followed by a first photoresist layer, followed by a transparent spacer layer, followed by a second photoresist layer with the pattern etched into it from the holographic fringe representation of an image, as required by claim 15. Therefore, the combination of *Taniguchi* and *Goto* does not teach each and every limitation of the invention claimed in claim 24. Applicant, therefore, respectfully requests that the rejection of claim 24 be withdrawn.

D. Claims 25-29

Claim 25 requires, "depositing a material layer over the photoresist layer ...." The Examiner asserts that the combination of *Taniguchi* and *Goto* renders claim 25 unpatentable. Neither *Taniguichi* nor *Goto* teach, or even suggest, depositing a material layer over a photoresist layer, as required by claim 25. Thus, *Taniguchi* and *Goto*, whether alone or in combination, does not teach each and every limitation of claim 25.

Claims 26–29 depend directly from independent claim 25 and therefore inherit all the elements of claim 25. Accordingly, claims 26–29 are allowable for at least the reasons discussed

above. Applicant, therefore, respectfully requests that the rejection of claims 25–29 likewise be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Thomas J. Meaney, Applicants' attorney, at 972-732-1001, so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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